

United States Patent and Trademark Office

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/836,104	04/17/2001	Yu-chun Chow	DEE-PT017	5930
34036 7.	590 09/21/2006		EXAMINER	
	LLEY PATENT GR	GREY, CHRISTOPHER P		
2350 MISSION COLLEGE BOULEVARD SUITE 360			ART UNIT	PAPER NUMBER
SANTA CLAR	A, CA 95054		2616	

DATE MAILED: 09/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

ST

	A					
	Application No.	Applicant(s)				
Office Action Summany	09/836,104	CHOW, YU-CHUN				
Office Action Summary	Examiner	Art Unit				
	Christopher P. Grey	2616				
The MAILING DATE of this communication app Period for Reply	ears on the cover sheet with the c	orrespondence address				
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).						
Status		•				
1) Responsive to communication(s) filed on 17 Ap	nril 2001					
·	action is non-final.					
<i>7</i>	, _					
	closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.					
	reparts quayro, 1000 C.D. 11, 10	0.0.210.				
Disposition of Claims						
4) Claim(s) <u>1-7</u> is/are pending in the application.						
4a) Of the above claim(s) is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>1-7</u> is/are rejected.						
7) Claim(s) is/are objected to.	7) Claim(s) is/are objected to.					
8) Claim(s) are subject to restriction and/or	election requirement.					
Application Papers						
9) The specification is objected to by the Examiner	:					
10) The drawing(s) filed on is/are: a) accepted or b) objected to by the Examiner.						
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).						
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
Priority under 35 U.S.C. § 119						
12)⊠ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a)⊠ All b)□ Some * c)□ None of:						
 2. Certified copies of the priority documents have been received in Application No 3. Copies of the certified copies of the priority documents have been received in this National Stage 						
application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received.						
See the attached detailed Office action for a list of the certified copies not received.						
Attachment(s)						
) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413)						
2) Notice of Draftsperson's Patent Drawing Review (PTO-948) Paper No(s)/Mail Date Disclosure Statement(s) (PTO/SB/08) Notice of Informal Patent Application						
Paper No(s)/Mail Date	6) Other:					
Patent and Trademark Office						

Art Unit: 2616

DETAILED ACTION

Page 2

Claim Objections

1. Claim 2 is objected to because of the following informalities:

In claim 2 line 3, "temporally" should be deleted, and replaced with, "temporarily" Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

- 2. Claim 1, 2, 3, 5 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by the prior art disclosed by the applicant
- Claim 1 The prior art disclosed by the applicant discloses a plurality of input/output ports for connecting said WAN and said LAN (fig 2, 112 and 121.

The prior art disclosed by the applicant discloses a buffer device (fig 2, 114 and 124 and page 1 line 25-27) for accessing packets, wherein a transporting path of the packets is selected from one of sending the packets from the WAN to the LAN and sending the packets from the LAN to the WAN (page 2 lines 4-6, routing).

Page 3

The prior art disclosed by the applicant discloses a plurality of medium access control units (fig 2, 112 and 122) corresponding to the input/output ports (fig 2, 111 and 121) and electrically connected between the buffer device (fig 2, 114 and 124) and the input/output ports for performing an accessing operation between the buffer device and the input/output ports (page 1, lines 23-27).

The prior art disclosed by the applicant discloses a memory device (fig 2, 16) electrically connected to the buffer device (fig 2, 114 and 124) for storing the packets sent from the buffer device (memory is electrically connected to buffer through the memory controller, internal bus and the internal bus controller, see fig 2).

The prior art disclosed by the applicant discloses a central processing unit fig 2, 17) electrically connected to the memory device (fig 2, 16) and the medium access control units (fig 2, 112 and 122) for processing the packets stored in the memory device (page 2 lines 4-6), and organizing the medium access control units to change the input/output ports according to a required transporting path (page 2, lines 4-6, CPU performs routing functions), thereby performing the communication between the LAN and WAN.

<u>Claim 2</u> The prior art disclosed by the applicant discloses a buffer (fig 2, 114 and 124) for temporarily storing the packets.

Art Unit: 2616

The prior art disclosed by the applicant discloses a buffer manager (fig 2, 113 and 123, controller) electrically connected to the buffer for managing an accessing operation of the buffer device (page 1 lines 25-27).

<u>Claim 3</u> The prior art disclosed by the applicant discloses a memory (fig 2,16) for storing the packets.

The prior art disclosed by the applicant discloses a memory controller (fig 2,15) electrically connected to the memory for controlling an accessing operation of the memory device (page 2 lines1-3).

<u>Claim 5</u> The prior art disclosed by the applicant discloses an internal bus (fig 2, 14) electrically connected to the memory controller (fig 2, 15) for transporting the packets.

The prior art disclosed by the applicant discloses a bus interface controller (fig 2, 115 and 125) electrically connected between the buffer device (fig 2, 114 and 124) and the internal bus (fig 2, 14) for controlling a transporting operation in the internal bus so as to complete a packet transporting operation between the buffer device and the internal bus (fig 2, and page 1 line 19-page 2 line16)

Claim 7 The prior art disclosed by the applicant discloses the central processing unit being used for processing the packets stored in the memory device to achieve functions of a router and a firewall (page 2 lines4-7).

Application/Control Number: 09/836,104 Page 5

Art Unit: 2616

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over the prior art disclosed by the applicant.

<u>Claim 4</u> The prior art disclosed by the applicant does not specifically disclose the memory being a DRAM.

It would have been obvious to one of the ordinary skill in the art at the time of the invention that the memory disclosed by the prior art disclosed by the applicant can be a variety of different types, where the use of DRAM is well known and applicable within the art, and is often used as opposed to SRAM because of its structural simplicity.

<u>Claim 6</u> The prior art disclosed by the applicant does not specifically disclose the buffer device, the medium access control units and the central processing unit being disposed in one identical chip.

It would have been obvious to one of the ordinary skill in the art at the time of the invention to have the CPU, MAC units and buffer all on the same chip. The motivation for how a chip set up is typically for cost and size benefits. Similarly, condensing the buffer, CPU and MAC units to one chip would reduce the cost by reducing the number of chips necessary.

Application/Control Number: 09/836,104

Art Unit: 2616

Conclusion

Page 6

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- (a) The applicant is urged to take a look at Zhang (US 6108345). Particularly, fig 3 depicts a number of the limitations within claim 1.
- 5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher P. Grey whose telephone number is (571)272-3160. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau Nguyen can be reached on (571)272-3126. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Christopher Grey Examiner

Art Unit 2616

CHAU NGUYEN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

Char Ti Nfigue

Sept 13 pro6